IMPERIAL COLLEGE LONDON

Design Engineering MEng EXAMINATIONS 2016

For Internal Students of the Imperial College of Science, Technology and Medicine
This paper is also taken for the relevant examination for the Associateship or Diploma

Engineering Analysis EA 1.3 - Electronics

Friday 24th June 2016 11.00 to 12.30

SOLUTIONS

This paper contains THIRTEEN questions.

Attempt ALL questions.

The numbers of marks shown by each question are for your guidance only; they indicate approximately how the examiners intend to distribute the marks for this paper.

This is a CLOSED BOOK Examination.

Q1 For the circuit shown in *Figure 1*, derive the equivalent resistance R_T between nodes A and B.

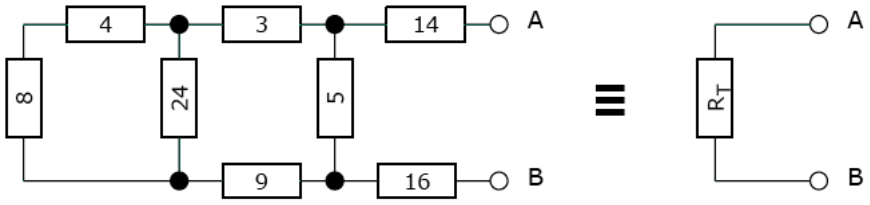


Figure 1

Solution

This question tests a student's ability to work on series and parallel combination of resistances, and the concept of "equivalency" in circuits.

$R_T = 14 + 16 + (((4 + 8) \parallel 24) + 3 + 9) \parallel 5 = 34\ k\Omega.$

[4]

(Most students managed to do this perfectly. Note that in the rubric, it says if a resistor is not explicitly labelled, it is in kΩ. Some students did not take notice of this and have the answer in ohms. No mark was deducted as a result.

For this question, one MUST work from left to right, gradually combining the resistors together. Knowing the formula for combining parallel resistors (i.e. produce-over-sum) is very helpful – it saves lots of time!

The average mark for this question was 3.4/4.0 or 90%.)

Q2. Use the method of voltage divider, find the value of V_1 for the circuit shown in *Figure 2*. Use the same method again, find the value of V_2.

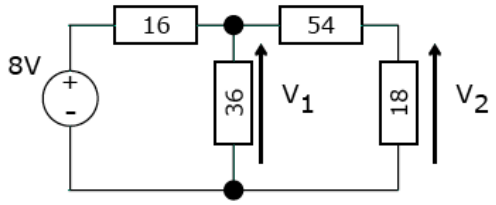


Figure 2

Solution

Combine 36 || (54 + 18) = 24. Therefore V1 =

8 * [24 /(24+16)] = 4.8V.

Now V1 is divided by the 54 and 18 resistors to get V2.

So V2 = 4.8 * [18/(18+54)] = 1.2V.

[6]

(Most common mistake made by students was to ignore the loading effect of the 54k and 18k resistors. They work out V1 using voltage divider principle only considering the 36k and 16k resistors, then use V1 value and the 18k and 54k as voltage dividers. In which case, I awarded 3 out of 6.

The average mark was 3.8 out of 6.0 or 63%.)

Q3. For the circuit shown in *Figure 3*, find the value of V_X with two different methods:

(a) By applying the principle of superposition;

(b) By employing nodal analysis.

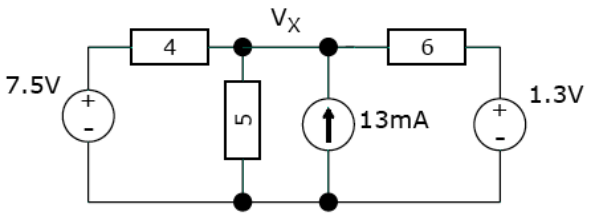


Figure 3

Solution

(a) Using superposition:

Vx due to 7.5V source: $7.5 * [(5 \parallel 6) / (5 \parallel 6 + 4)] = 3$
Vx due to 13mA source: $13 * (4 \parallel 5 \parallel 6) = 21.1$
Vx due to 1.3V source: $1.3 * [(4 \parallel 5) / (4 \parallel 5 + 6)] = 0.35$

Therefore Vx (total) = 24.5V.

[5]

(b) Using nodal analysis:

Applying KCL at node Vx

$(Vx - 7.5)/4 + Vx/5 + (Vx-1.3)/6 = 13 \Rightarrow Vx = 24.5V.$

[5]

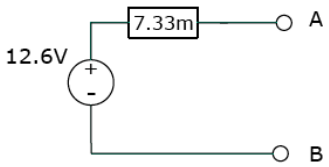
(The most common mistake is to zero one of the sources instead of all except one. Most showed some appreciation of how to use principle of superposition and nodal analysis using KCL.
Note that in the rubric, it says if a resistor is not explicitly labelled, it is in kΩ. Some students did not take notice of this and have the answer in ohms. Some student use ohm instead of kilo ohms. I also made the mistake of explicitly say the current is in mA. I should have omitted the unit mA, then it would not have mattered whether student use kΩ and mA, or ohms and A. My bad! I did not deduct any mark if student assume any combination and got the method correct.
The tricky bit of this question is to have three sources. Nevertheless quite a few students got the perfect answer for this question.
Average mark: 8.3 out of 10, or 83%.)

Q4. (a) A car battery has an open-circuit terminal voltage of 12.6V. The terminal voltage drops to 11.5V when the battery supplies 150A to a starter motor. What is the Thévenin equivalent circuit of this battery?

(b) On a cold morning, the starter motor draws 240A of current while starting the car. What is the minimum terminal voltage of the battery?

Solution

(a)



V_{TH} = 12.6V and R_{TH} = 7.33 mΩ.

[3]

(b)

$V_{battery}$ = 10.84V.

[3]

(I thought this is a really nice question that separate those who truly understood Thevenin equivalent circuits, and those who don't. Many got this perfectly, and some had no clue!

The average mark: 3.7 out of 6, or 62%. It is actually a really easy question.)

Q5. In the circuit shown in *Figure 5*, the switch remains in position 1 (i.e. closed) for a long time before moving to position 2 (i.e. open) at time $t = 0$ s. Find:

(a) the capacitor voltage $v_C(t)$ at $t = 0$ s before the switch is open;

(b) the final value of v_C for $t \to \infty$;

(c) the time constant of the function $v_C(t)$ for $t \geq 0$ s, and;

(d) an equation for v_C as a function of time t.

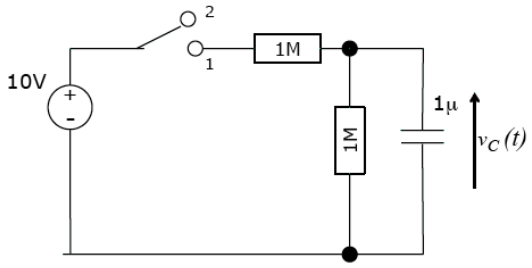


Figure 5

Solution

(a) $v_C(0) = 5$V (simple voltage divider.

[2]

(b) $v_C(t \to \infty) = 0$V because capacitor will eventually discharge all its stored charge.

[2]

(c) Time constant $\tau = 10^6 \times 10^{-6} = 1$ second.

[2]

(d) Using the initial and final value theorem:

$$v_C(t) = v_C(0) + (v_C(\infty) - v_C(0))(1 - e^{-\frac{t}{\tau}})$$

[2]

(This question is one that one can either do it or can't. I would have thought that after Lab2, everyone should have mastered this type of questions. For a) many gave 10V as the answer not seeing that when the switch is close, the two resistors act as voltage divider. This shows those who call really "see" a circuit, and those that blindly apply formulae. Average mark: 5.0 out of 8.0, or 63%.)

Q6 Express the voltage $v_S\ (t) = 4cos2t$ in phasor form (i.e. magnitude and phase) and as complex source. For the circuit shown in *Figure 6*, compute the combined impedance Z_T of the capacitor and the inductor. Hence derive the voltage *v(t)* as a phasor and then as a function in time.

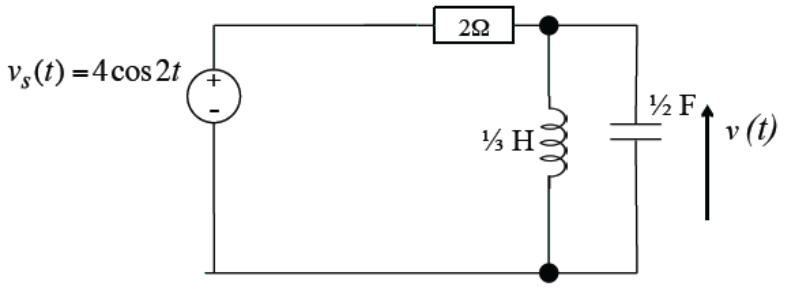


Figure 6

Solution

$v_S\ (t) = 4cos2t$ in phasor form: $\bar{V}_S = 4\angle 0^\circ$ and in complex value: 4 + 0j.

$Z_L = j\,\omega L = j\ 2/3$ $\quad Z_C = 1/j\,\omega C = -j$ $\quad Z_T = \frac{\frac{2}{3}}{-\frac{1}{3}j} = 2j$

Therefore,

$$\bar{V} = \frac{Z_T}{Z_T + 2}\bar{V}_S = \frac{2j}{2 + 2j} \times (4 + 0j) = \frac{4j}{1 + j} = 2(1 + j)$$

Hence:

$$\bar{V} = 2\sqrt{2}\angle 45^\circ$$

and $$v(t) = 2\sqrt{2}\cos(2t + \tfrac{\pi}{4})$$

[10]

(This question turned out to be much harder than I expected and most students only got it partially correct and some had no clue as to what to do. Nevertheless a couple of students got 100%! I think I need to remove phasor and just use complex analysis for impedances in the future.
Average marks: 4.5 out of 10, or 45%.)

Q7. For the RC circuit shown in *Figure 7*:

(a) determine the frequency response function $H(j\omega) = V_o(j\omega) / V_i(j\omega)$.

(b) Given that R = 1kΩ and C = 1nF, determine the amplitude response $|H(j\omega)|$ at the frequency $\omega = 1/RC$.

(c) For this circuit, sketch the amplitude $|H(j\omega)|$ versus frequency.

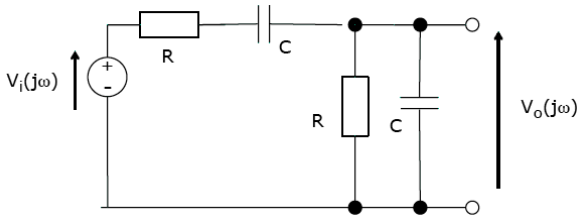


Figure 7

S

Solution

(a)

$$H(j\omega) = \frac{Z_2}{Z_1 + Z_2} = \frac{1}{1 + Z_1 Y_2} = \frac{1}{1 + (R + \frac{1}{j\omega C})(j\omega C + \frac{1}{R})}$$

$$= \frac{j\omega RC}{1 + j3\omega RC - (\omega RC)^2}$$

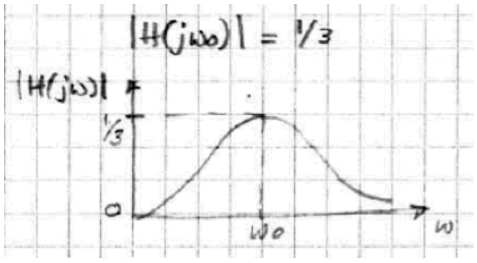
[6]

(b)

$H(j\omega) = \frac{j}{1+3j-1^2} = 1/3.$ Hence at $\omega RC = 1$. Amplitude is 1/3.

[4]

(c)



[4]

(This question turned out to be really difficult for most students. Even those who could do it took a lot of time. Having TWO capacitors instead of one makes it really hard.
However, one student managed to get the perfect score for this, demonstrating that it is do-able!
Next time, I will choose a simpler circuit than this one.
Average mark: 4.9 out of 14 or 35% - this quite low!)

Q8. The circuit in *Figure 8* contains two operational amplifiers with ideal characteristics. All resistors are of value R. Determine the voltages v_1 and v_2, and the output gain vo/v_S.

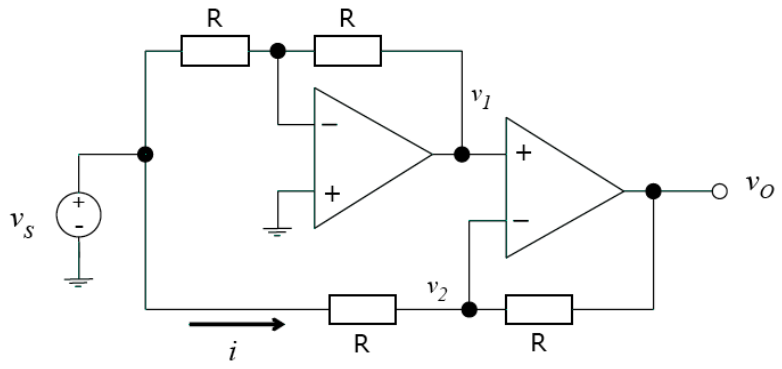


Figure 8

Solution

The top opamp is a simple inverting unity gain amplifier. Therefore $v_1 = -v_S$. Therefore v_2 is also $-v_S$.

Current i is $(v_2 - v_S)/R = -2\ v_S\ /R$. Since the current must flow in the feedback resistor of the right opamp,

$vo = v2 - iR \Rightarrow vo = -\ v_S - 2\ v_S = -3\ v_S$, Hence the gain = -3.

[8]

(Around half of the class could do this question well and another half got only a bit of it. I awarded 4 out of 8 if they can work out the gain of the inverting and the non-inverting paths, but could not combine them together using superposition principle. It is not a difficult question, but really separate those who truly understood and those who did not. Average mark: 4.5 out of 8.0, or 56%.)

Q9 Figure 9 shows a single power supply operational amplifier being driven by a source voltage $v_S(t)$. Explain the purpose of each of the three capacitors in the circuit. Derive the equation for the output voltage $v_O(t)$. State any assumption used.

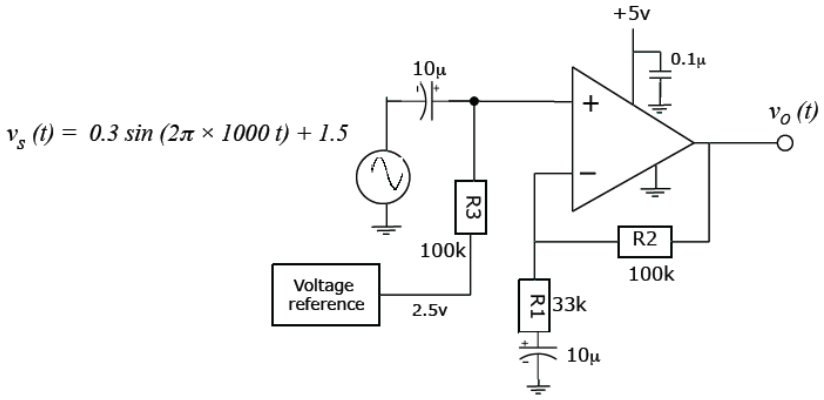


Figure 9

Solution

The 10µF capacitors are to provide AC coupling and remove the DC. The gain of the amplifier is (1+R2/R1) = 4 for all frequency >> 1/(2π RC) or 0.5Hz.

The voltage reference provide offset of 2.5v at output. Therefore

$$v_O(t) = 2.5 + 1.2 \sin(2\pi \times 1000t)$$

Assumptions are: the voltage reference has zero dynamic impedance, the opamp is ideal and finally the output voltage range is 0 v to 5v, i.e. the output swing does not cause saturation.

[8]

(This question was directly linked to Lab 3 – it was intentional so that those who did Lab 3 and understood it could gain at least 4 out of 8 in answering the first part of the question – the only part that is descriptive in this paper.
The second part is somewhat more challenging and only a few students got the correct answer.
Average mark: 3.6 out of 8, or 45%. It is lower than I expected.)

Q10. Given that the decimal code for the ASCII character 'A' is 65, and assuming that all numbers are represented using 8 bits, complete the missing entries that are not shaded in the following table. (No marks will be awarded for this question unless you show how the solutions are derived.)

Solution

Binary	Hexadecimal	Unsigned Decimal	ASCII
10011011	**9B**	**155**	
0100 0111		71	**'G'**

[8]

(This perhaps the easiest question of the entire paper. Really straight forward.
Average mark: 6.6 out of 8.0, or 82%.)

Q11. A microcontroller board has a built-in 12-bit analogue-to-digital converter (ADC) that accept an input voltage ranging from 0 to 3.3V. Assuming that the conversion accuracy is ±½ LSB, what is the voltage resolution and accuracy of this ADC?

Solution

Range is 3.3V. 12-bits results in 4096 quantization steps. Therefore the resolution, i.e. voltage per LSB = 3.3V/4096 = 0.8mV.

Accuracy is half that, which is ±0.4mV.

[4]

(This should have been a really easy question, but many students did not even attempt it. I think I need to elaborate on the idea of accuracy and resolution more next year in my lectures. There was also no tutorial problem on ADC and DAC – something that I need to fix for next year.
Average mark: 0.4 out of 4.0, or 10%.)

Q12. Simplify the following Boolean expressions using De Morgan's theorem and Boolean algebra.

i) $\overline{A \bullet \left(B + \overline{C}\right) \bullet D}$

ii) $\left(P + \overline{Q}\right) \bullet \left(\overline{P} + Q\right)$

Solution

i) $\overline{A \bullet \left(B + \overline{C}\right) \bullet D} = \overline{A \bullet \left(\overline{B} \bullet C\right) \bullet D} = \overline{A} + B + \overline{C} + \overline{D}$

ii) $\left(P + \overline{Q}\right) \bullet \left(\overline{P} + Q\right) = \overline{P} \bullet Q + P \bullet \overline{Q} = P \oplus Q$

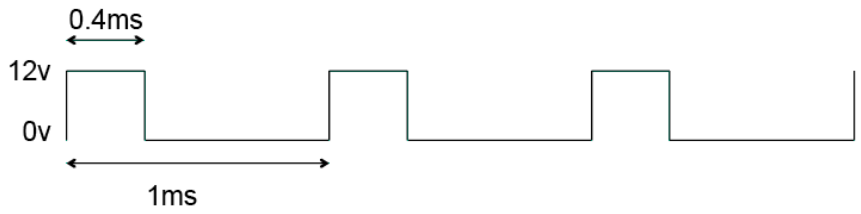
[8]

(This is also an easy question. However some student did not revise or did not understand De Morgan theorem. If they do, it is really really easy to get full marks. Any answer showing that he/she understood De Morgan and can apply this to the Boolean equations were given full marks.
Average mark: 5.9 out of 8.0, or 74%.)

Q13 A dc motor is controlled by a microcontroller using pulse-width modulation (PWM). The PWM signal is running at 1kHz and is interfaced to the motor via a motor driver chip which has supply voltage of 12 volts. It is known that the maximum motor speed is 500 rpm at 12V. Sketch the drive signal to the motor indicating all voltages and time if the motor is running at 200 rpm. State any assumption used.

Solution

Assuming that the speed varies linearly with the average of the drive voltage, 200 rpm is 40% of full speed. Therefore the PWM signal must be at 40% duty cycle. The signal must be:



[6]

(Given that students should have been familiar with PWM principle and therefore should know the answer with minimal effort, I was disappointed that many had no clue how to draw the waveform. Not that exactly where the pulse is positioned is not important. It is the mark-space ratio that matters. Many did not even attempt this at all! Those who could do it got full marks.
Average mark: 2.3 out of 6.0 or 38%.)

Overall Remarks:

I think this paper is hard and it is also a bit long. A small number of students managed to do all questions, but many did not have time to attempt 3 to 5 questions. Next year, I will reduce the number of questions and NOT cover the whole syllabus (as I attempt to do in this paper).

Since students really engaged in the Labs and the Project, the average marks of the coursework components which contributes 40% to the final mark had a high average of 70.3%. Therefore a more challenging examination paper is not a bad thing. In the end, students scored an average of 57% on this exam paper. This made the total average for EA1.3 a very respectable 62.3%.

Overall the paper did separate those who were good in electronics and those who were not. Every single question had someone who score full marks and someone who score near to zero. Therefore it is a fair test of the learning outcome of students. However, I think I should reduce the number of questions next year, so that most students would not run out of time.

The grade distribution of the final module marks was near perfect: A – 20%, B – 40%, C – 35% and D – 5%. Well-done class.